REMARKS

Claims 1-17 are pending in this application.

Claims 1-17 have been rejected.

No claims have been allowed.

Claim 1 has been amended as shown above. Because this amendment places Claim 1 in better condition for allowance or appeal and does not narrow the scope of Claim 1, this amendment complies with 37 C.F.R. § 1.116.

Reconsideration of the claims is respectfully requested.

I. 35 U.S.C. § 102(e) – Anticipation

The Office Action rejects Claims 1-4, 11-13, and 17 under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,233,637 issued to Smyers et al. ("*Smyers*"). This rejection is respectfully traversed.

A cited prior art reference anticipates the claimed invention under 35 U.S.C. § 102 only if every element of a claimed invention is identically shown in that single reference, arranged as they are in the claims. MPEP § 2131; *In re Bond*, 910 F.2d 831, 832, 15 U.S.P.Q.2d 1566, 1567 (Fed. Cir. 1990). Anticipation is only shown where each and every limitation of the claimed invention is found in a single cited prior art reference. MPEP § 2131; *In re Donohue*, 766 F.2d 531, 534, 226 U.S.P.Q. 619, 621 (Fed. Cir. 1985).

Smyers recites a system for providing a bi-directional path between an application and a data bus. (*Abstract*). The system includes an isochronous data pipe and an asynchronous data

pipe, and each data pipe includes a register set. (*Col. 3, Lines 30-43*). The register sets (elements 24 and 28) are programmed by the application. (*Col. 4, Lines 47-48*). The register sets contain information controlling how a data transfer should occur in the asynchronous data pipe and defining how data is to be processed in the isochronous data pipe. (*Col. 4, Lines 47-50; Col. 11, Lines 49-53*). The system also includes a set of control registers (element 38). (*Col. 3, Lines 38-43*).

Smyers does not anticipate "register transfer units" that "facilitate transfers of data among at least two interface registers" as recited in Claim 1.

First, the Office Action asserts that *Smyers* recites this element at column 3, line 64 through column 4, line 7. (*Office Action, Page 3, Second paragraph*). However, this portion of *Smyers* recites using First In, First Out (FIFO) queues to transport information between the data pipes (elements 20 and 26) and a link core (element 44).

Smyers contains no recitation that the FIFO queues are used to transport information between registers. In particular, the FIFO queues do not transport data between the control registers (element 38). Also, the register sets (elements 24 and 28) contain information controlling how a data transfer should occur in the asynchronous data pipe and defining how data should be processed in the isochronous data pipe. *Smyers* contains no recitation that the contents of the registers in one register set are transported to registers in another register set. As a result, the FIFO queues recited in *Smyers* do not anticipate a "plurality of register transfer units" that "facilitate transfers of data among interface registers" as recited in Claim 1.

Second, the Office Action asserts that *Smyers* discloses "transferring data between the registers in the data pipes" at column 12, line 28 through column 13, line 65. (*Office Action, Page 8, Paragraph 8*). However, this portion of *Smyers* describes the register set of the isochronous data pipe. (*Col. 11, Lines 49-53*). As a result, any transfer of data between registers in this register set occurs only within the isochronous data pipe, not between the two data pipes.

Moreover, this portion of *Smyers* refers to three different registers: a "current stack register" (*Col. 12, Lines 28-37*), a "source register" (*Col. 12, Lines 54-56*), and a "destination register" (*Col. 12, Lines 56-58*). There is no recitation in *Smyers* that any of these registers are "operably coupled" to one or more "interface registers" as recited in Claim 1. There is also no recitation in *Smyers* that any of these registers "facilitate transfers of data among at least two interface registers" as recited in Claim 1.

Smyers simply recites the use of two data pipes, where the data pipes operate under the control of register sets. *Smyers* lacks any mention of "register transfer units" that "facilitate transfers of data among at least two interface registers" as recited in Claim 1. As a result, *Smyers* fails to anticipate the Applicants' invention as recited in Claim 1 (and Claims 2-5 depending from Claim 1). For similar reasons, *Smyers* fails to anticipate the Applicants' invention as recited in Claim 11 (and Claims 12-17 depending from Claim 11).

Accordingly, the Applicants respectfully request withdrawal of the § 102(e) rejection and full allowance of Claims 1-4, 11-13, and 17.

II. 35 U.S.C. § 103(a) – Obviousness

The Office Action rejects Claims 5-10 and 14-16 under 35 U.S.C. § 103(a) as being unpatentable over *Smyers* in view of "Applicant Admitted Prior Art" ("*AAPA*"). This rejection is respectfully traversed.

Claim 5 depends from Claim 1, and Claims 14-16 depend from Claim 11. *Smyers* fails to disclose, teach, or suggest the Applicants' invention as recited in Claims 1 and 11. As a result, Claims 5 and 14-16 are allowable due to their dependence from allowable base claims.

Regarding Claims 6-10, *Smyers* fails to disclose, teach, or suggest a "plurality of register transfer units" that facilitate "transfers of data among interface registers" as recited in Claim 6. The Office Action only relies on the *AAPA* as reciting a channel decoder. The Office Action does not cite the *AAPA* as reciting a "plurality of register transfer units" that facilitate "transfers of data among interface registers." As a result, the proposed *Smyers-AAPA* combination fails to disclose, teach, or suggest the Applicants' invention as recited in Claim 6 (and Claims 7-10 depending from Claim 6).

Accordingly, the Applicants respectfully request withdrawal of the § 103(a) rejection and full allowance of Claims 5-10 and 14-16.

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SUMMARY

For the reasons given above, the Applicants respectfully request reconsideration and allowance of pending claims and that this application be passed to issue. If any outstanding issues remain, or if the Examiner has any further suggestions for expediting allowance of this application, the Applicants respectfully invite the Examiner to contact the undersigned at the telephone number indicated below or at *wmunck@davismunck.com*.

The Commissioner is hereby authorized to charge any additional fees connected with this communication or credit any overpayment to Davis Munck Deposit Account No. 50-0208.

Respectfully submitted,

DAVIS MUNCK, P.C.

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William A. Munck
Registration No. 39,308

P.O. Drawer 800889
Dallas, Texas 75380
Phone: (972) 628-3600
Fax: (972) 628-3616
E-mail: wmunck@davismunck.com